

## Claims

What is claimed is:

- 1           1.     A method for implementing enhanced performance with  
2 reduced quiescent power dissipation using mixed threshold CMOS devices  
3 in latch circuit designs comprising the steps of:  
4           identifying logic blocks in critical data and clock paths of a latch  
5 circuit;  
6           substituting a low voltage threshold (LVT) transistor to replace each  
7 regular voltage threshold (RVT) transistor for use in said identified logic  
8 blocks in the critical data and clock paths; and  
9           selectively implementing non-critical sections of the latch circuit with  
10 RVT transistors, or low leakage (LLD) transistors.
- 1           2.     A method for implementing enhanced performance with  
2 reduced quiescent power dissipation as recited in claim 1 includes the steps  
3 of providing RVT transistors to implement output buffer transistors.
- 1           3.     A method for implementing enhanced performance with  
2 reduced quiescent power dissipation as recited in claim 1 wherein the step of  
3 identifying logic blocks in critical data and clock paths of the latch circuit  
4 includes the steps of identifying logic blocks used in loading data into the  
5 latch circuit.
- 1           4.     A method for implementing enhanced performance with  
2 reduced quiescent power dissipation as recited in claim 3 includes the steps  
3 of identifying logic blocks used in each data clock stage.
- 1           5.     A method for implementing enhanced performance with  
2 reduced quiescent power dissipation as recited in claim 1 wherein the step of  
3 selectively implementing non-critical sections of the latch circuit with RVT  
4 transistors, or low leakage (LLD) transistors includes the steps of identifying  
5 logic blocks used only during testing in the latch circuit; and selectively  
6 implementing the identified logic blocks used only during testing with RVT  
7 transistors, or low leakage (LLD) transistors.

1           6.     A method for implementing enhanced performance with  
2 reduced quiescent power dissipation as recited in claim 1 wherein the step of  
3 selectively implementing non-critical sections of the latch circuit with RVT  
4 transistors, or low leakage (LLD) transistors includes the steps of identifying  
5 logic blocks used to maintain the contents of latches in the latch circuit; and  
6 selectively implementing the identified logic blocks used to maintain the  
7 contents of latches with RVT transistors, or low leakage (LLD) transistors.

1           7.     A latch circuit for implementing enhanced performance with  
2 reduced quiescent power dissipation comprising:  
3           critical data and clock paths;  
4           non-critical sections;  
5           a low voltage threshold (LVT) transistor being used only in said critical  
6 data and clock paths; and  
7           said non-critical sections being implemented with regular voltage  
8 threshold (RVT) transistors, or low leakage (LLD) transistors.

1           8.     A latch circuit for implementing enhanced performance with  
2 reduced quiescent power dissipation as recited in claim 7 includes said RVT  
3 transistors used for output buffer transistors.

1           9.     A latch circuit for implementing enhanced performance with  
2 reduced quiescent power dissipation as recited in claim 7 wherein said  
3 critical data and clock paths include multiple critical path logic blocks, each  
4 critical path logic block implemented with said LVT transistors.

1           10.    A latch circuit for implementing enhanced performance with  
2 reduced quiescent power dissipation as recited in claim 7 wherein said non-  
3 critical sections include logic blocks used for testing and to maintain the  
4 contents of latches in the latch circuit.

1           11.    A computer program product for implementing enhanced  
2 performance with reduced quiescent power dissipation using mixed  
3 threshold CMOS devices in latch circuit designs in a computer system, said  
4 computer program product including instructions executed by the computer  
5 system to cause the computer system to perform the steps of:

6                identifying logic blocks in critical data and clock paths of a latch  
7 circuit;

8                substituting a low voltage threshold (LVT) transistor to replace each  
9 regular voltage threshold (RVT) transistor for use in said identified logic  
10 blocks in the critical data and clock paths; and

11               selectively implementing non-critical sections of the latch circuit with  
12 RVT transistors, or low leakage (LLD) transistors.

1           12.    A computer program product for implementing enhanced  
2 performance with reduced quiescent power dissipation as recited in claim 11  
3 includes the steps of providing RVT transistors to implement output buffer  
4 transistors.

1           13.    A computer program product for implementing enhanced  
2 performance with reduced quiescent power dissipation as recited in claim 11  
3 wherein the step of identifying logic blocks in critical data and clock paths of  
4 the latch circuit includes the steps of identifying logic blocks used in loading  
5 data into the latch circuit.

1           14.    A computer program product for implementing enhanced  
2 performance with reduced quiescent power dissipation as recited in claim 13  
3 includes the steps of identifying logic blocks used in a data clock stage.

1           15.    A computer program product for implementing enhanced  
2 performance with reduced quiescent power dissipation as recited in claim 11  
3 wherein the step of selectively implementing non-critical sections of the latch  
4 circuit with RVT transistors, or low leakage (LLD) transistors includes the  
5 steps of identifying logic blocks used only during testing in the latch circuit;  
6 and selectively implementing the identified logic blocks used only during  
7 testing with RVT transistors, or low leakage (LLD) transistors.

1           16.    A computer program product for implementing enhanced  
2 performance with reduced quiescent power dissipation as recited in claim 11  
3 wherein the step of selectively implementing non-critical sections of the latch  
4 circuit with RVT transistors, or low leakage (LLD) transistors includes the  
5 steps of identifying logic blocks used to maintain the contents of latches in  
6 the latch circuit; and selectively implementing the identified logic blocks used  
7 to maintain the contents of latches with RVT transistors, or low leakage  
8 (LLD) transistors.